

## Abstract

A semiconductor device for comparing an input address with a repair address includes a signal controller for  
5 generating control signals. An address latch unit in response to the control signals latches the address. Each of N number of M-bit address comparators compares the address with the stored repair address. A comparator delay modeling block delays the control signal for a predetermined time, i.e.,  
10 delay value of the M-bit address comparator. A repair circuit controller in response to the delayed control signal output from the comparator delay modeling block generates one of a repair address enable signal and a normal address enable signal based on a comparison result of the M-bit address  
15 comparator.